REMARKS

Claims 21-24 stand rejected as of the Office Action dated October 16, 2002. Claims 21 and 22 were amended. No new matter was added. Reconsideration of pending claims 21-24 is respectfully requested in light of the amendments and the following remarks.

Claim Rejections – 35 USC § 112

Claim 22 was rejected under 35 USC § 112, second paragraph, as being indefinite. Claim 22 is henceforth amended to recite "silicon nitride (SiN)" rather than "silicon oxide (SiN)". This amendment is supported by the application on page 6, lines 15-16. Thus, the claim 22 rejection under this section is overcome.

Claim Rejections – 35 USC § 102

Claim 21 was rejected under 35 USC § 102(e) as being anticipated by US Patent No. 6,396,092 issued to Takatani et al. ('Takatani'). The applicant disagrees with this rejection for the following reasons.

Claim 21 recites, in part, "a blocking layer formed on the buried contact structure and the first interlayer insulating layer." In his remarks concerning claim 21, the Examiner has compared Takatani's item 41 (FIG. 7) and Takatani's item 52 (FIGS. 8-10) to the applicant's blocking layer and buried contact structure, respectively. However, a closer inspection of Takatani FIGS. 5-10 shows that his "blocking layer" 41 is not formed on the "buried contact structure" 52 like applicant's blocking layer 214 (FIG. 2) is formed on applicant's buried contact structure 212b (FIG. 2; FIG. 3D, page 11, lines 10-18).

Furthermore, claim 21 originally recited, in part, "a ferroelectric capacitor electrically connected to the buried contact structure through a second contact hole." Claim 21 is amended to recite, in part, "a ferroelectric capacitor that fills a second contact hole and connects to the buried contact structure through the second contact hole." This amendment is supported by FIG. 2 and the application at page 8, lines 3-28. Applicant's FIG. 2 shows that the lower electrode 220 of the capacitor 226 is directly connected, and not just electrically connected, to the buried contact structure 212b through the second contact hole 218. Conversely, Takatani's "lower electrode" 61 (FIG. 10) does not connect to the "buried contact structure" 52 through the second contact hole, but rather it connects to the "buried contact structure" 52 *at the surface* of the second contact hole (FIG. 10, emphasis added). In

other words, Takatani's "lower electrode" 61 does not fill the second contact hole like the applicant's lower electrode 220 (FIG. 2).

Thus, applicant submits that the § 102(e) rejection to claim 21 is overcome because Takatani does not disclose each and every element of the recited claim.

Claim Rejections – 35 USC § 103

Claims 21, 22, and 23 were rejected under 35 USC § 103(a) as being unpatentable over US Patent No. 6,329,680 issued to Yoshida et al. ('Yoshida') in view of US Patent No. 5,411,911 issued to Ikeda et al. ('Ikeda'). The applicant disagrees because even if there was a suggestion or motivation to combine the two references, the resulting combination does not teach or suggest all the claim limitations. Thus, as explained below, prima facie obviousness has not been established.

With regard to claim 21, applicant claims, in part, a first interlayer insulating layer formed on a semiconductor substrate. The application discloses a single insulating layer composed of only one material (FIG. 2). The Examiner has improperly equated the applicant's homogenous first interlayer insulation layer to Yoshida's multiple-layer structure of silicon oxide film and spin-coated SOG (spin on glass) film that requires multiple distinct fabrication processes (items 37, 38, and 39 - FIG. 5; column 7, lines 3-15).

Even if one of Yoshida's layers 37, 38, or 39 is accepted as equivalent to the claimed first interlayer insulating layer, the rest of the comparison would fail. It is impossible for either of Yoshida's single layers 37 or 39 to both be formed on (touching – see FIG. 2) the semiconductor substrate and have a buried contact structure formed on (touching – see FIG. 2) the single layer 37 or 39.

Finally, claim 21 is amended to recite, in part, "a ferroelectric capacitor that fills a second contact hole and connects to the buried contact structure through the second contact hole." This amendment is supported by FIG. 2 and the application at page 8, lines 3-28. Previously, claim 21 recited, in part, "a ferroelectric capacitor electrically connected to the buried contact structure through a second contact hole." Applicant's FIG. 2 shows that the lower electrode 220 of the capacitor 226 is directly connected, and not just electrically connected, to the buried contact structure 212b through the second contact hole 218. Conversely, Yoshida's "lower electrode" 59 does not directly contact the "buried contact structure" through the "second contact hole" 52, but rather it is electrically connected to the "plug" 53 that fills the "second contact hole" 52 (column 8, lines 65-66; FIG. 5).

For at least these reasons, claim 21 is allowable over the combination of Yoshida and Ikeda because together they fail to teach all the limitations of claim 21.

With regard to claim 22, since claim 21 is its parent it should be allowable for at least the same reasons given above with respect to claim 21.

With regard to claim 23, it is dependent upon claim 21 and should be allowable for at least the same reasons as claim 21.

Claim 24 was rejected under 35 USC § 103(a) as being unpatentable over Yoshida in view of Ikeda and further in view of US Patent Application Publication No. 2002/0011615 filed by Nagata et al. ('Nagata'). Yoshida remains deficient in the manner outlined above for claim 21, regardless of what Nagata may or may not teach about the interchangeability of polysilicon and tungsten. Thus, because the combination of Yoshida and Nagata fails to suggest all the limitations inherent to claim 24, claim 24 is patentable over Yoshida and Nagata.

Conclusion

For the foregoing reasons, reconsideration and allowance of claims 21-24 of the application as amended is solicited. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

21. (Amended) A ferroelectric memory device comprising:

a first interlayer insulating layer formed on a semiconductor substrate;

a buried contact structure electrically connected to the substrate through a first contact hole extending through the first interlayer insulating layer, the buried contact structure formed on the first interlayer insulating layer;

a blocking layer formed on the buried contact structure and the first interlayer insulating layer;

a second interlayer insulating layer formed on the blocking layer; and

a ferroelectric capacitor that fills a second contact hole and [electrically connected] connects to the buried contact structure through [a] the second contact hole that penetrates the second interlayer insulating layer and the blocking layer, the ferroelectric capacitor being formed on the second interlayer insulating layer.

22. (Amended) The ferroelectric memory device according to claim 21, wherein the blocking layer comprises silicon oxynitride (SiON), silicon [oxide] nitride (SiN), or aluminum oxide to prevent oxygen diffusion.